

CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

17CS72

Seventh Semester B.E. Degree Examination, Jan./Feb. 2023 Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. What are Performance factors? How system attributes affects on Performance factors? Explain. (08 Marks)
b. Explain the Architecture of the Vector Super Computer, with diagram. (07 Marks)
c. Explain the Flynn's classification briefly. (05 Marks)

OR

- 2 a. What is Data Dependence? Explain types of Data dependence with dependency graph. (08 Marks)
b. Explain Static Interconnection Networks with examples. (07 Marks)
c. What are the metrics affecting the scalability of Computer Architecture? Explain. (05 Marks)

Module-2

- 3 a. With diagram, explain the basic architecture of the scalar computers. (08 Marks)
b. Distinguish Architectures between CISC and RISC computers, with neat diagram. (05 Marks)
c. What is Super Scalar Architecture? Explain the superscalar RISC processor architecture. (07 Marks)

OR

- 4 a. With diagram, explain the hierarchy of the Memory Technology. (05 Marks)
b. Explain the Inclusion property and locality of reference along with its type in Memory hierarchy. (07 Marks)
c. Explain TLB, Paging and Segmentation. (08 Marks)

Module-3

- 5 a. What is Bus Arbitration? Explain distributed Bus Arbitration. (07 Marks)
b. Explain Cache Memory modes with neat diagram. (08 Marks)
c. Explain Sequential Consistency Memory Model. (05 Marks)

OR

- 6 a. Explain Speedup, Efficiency and through put of Linear Pipeline Processors. (05 Marks)
b. Consider the reservation table given below and determine the
i) For bidden latencies ii) MAL iii) Initial collision vector and
iv) Stat diagram for the non-linear pipeline. (07 Marks)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- c. What are Instruction Pipeline Processors? Explain Pipeline design multiplication 8 – bit arithmetic, with diagram. (08 Marks)

Module-4

- 7 a. What are the Dynamic Interconnect Networks? Explain Routing in Dynamic OMEGA 8×8 Interconnect Network using 2×2 switch modules. (08 Marks)
 b. What is Vector Processing? Explain Vector schemes and memory with diagram. (07 Marks)
 c. Write a note on Cross Bar Networks design V/s Multiport Memory. (05 Marks)

OR

- 8 a. Explain Hierarchical Bus System with diagram. (05 Marks)
 b. Explain four Context – Switching Policies in Multiprocessing Modes. (08 Marks)
 c. Explain Connection Machine CM – 2 Architecture, with diagram. (07 Marks)

Module-5

- 9 a. Define Parallel Programming Model. Explain shared and distributed parallel models. (08 Marks)
 b. Explain Concurrent OOP and Actor model in Object Oriented Parallel Programming Model. (05 Marks)
 c. Explain principles of Synchronization in Parallel Programming in Multiprocessing. (07 Marks)

OR

- 10 a. With the help of neat diagram, explain Computation phases in code generation in parallel computation. (07 Marks)
 b. Explain different language features of Parallel programming. (08 Marks)
 c. Write a note on Dependency Testing. Briefly. (05 Marks)
